奇美電子
CHIMEI INNOLUX

PRODUCT SPECIFICATION

□Tentative Specification
□Preliminary Specification
■Approval Specification

MODEL NO.: V315HK2
SUFFIX: PE1

Customer:

APPROVED BY   **SIGNATURE**

Name / Title _____   _____
Note

_____

Please return 1 copy for your confirmation with your
signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Josh Chi	**Edouard Huang**

Version 2.0   **1**   **Date：7 Dec 2010**

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Dec. 7, 2010	All	All	The Approval specification was first issued.

PRODUCT SPECIFICATION

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315HK2-PE1 is a 31.5" TFT Liquid Crystal Display product with driver ICs and 4ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 1.07G (8-bit+Hi-FRC)colors. The backlight unit is not built in.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	31.51
Pixels [lines]	1920 x 1080
Active Area [mm]	698.4 (H) x 392.85 (V) (31.51" diagonal)
Sub-Pixel Pitch [mm]	0.12125 (H) x 0.36375 (V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	1175
Physical Size [mm]	716.1(H)X410.0 (V) $\times$ 1.8(D) Typ.
Display Mode	Transmissive mode / Normallly black
Contrast Ratio	6000:1 Typ. (Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR$\geq$20) (Typical value measure at CMI's module)
Color Chromaticity	R = (0.654, 0.325) G = (0.266, 0.591) B = (0.131, 0.115) W= (0.301, 0.357) Standard light source "C"
Cell Transparency [%]	4.5%Typ.. (Typical value measured at CMO's module)
Polarizer Surface Treatment	Super clear coating, Hard coating (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight		1175		g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within $\pm$ 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

Note (1) Temperature and relative humidity range is shown in the figure below.

   (a) 90 %RH Max. (Ta $\leqq$ 40 ºC).

   (b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

   (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Relative Humidity (%RH)
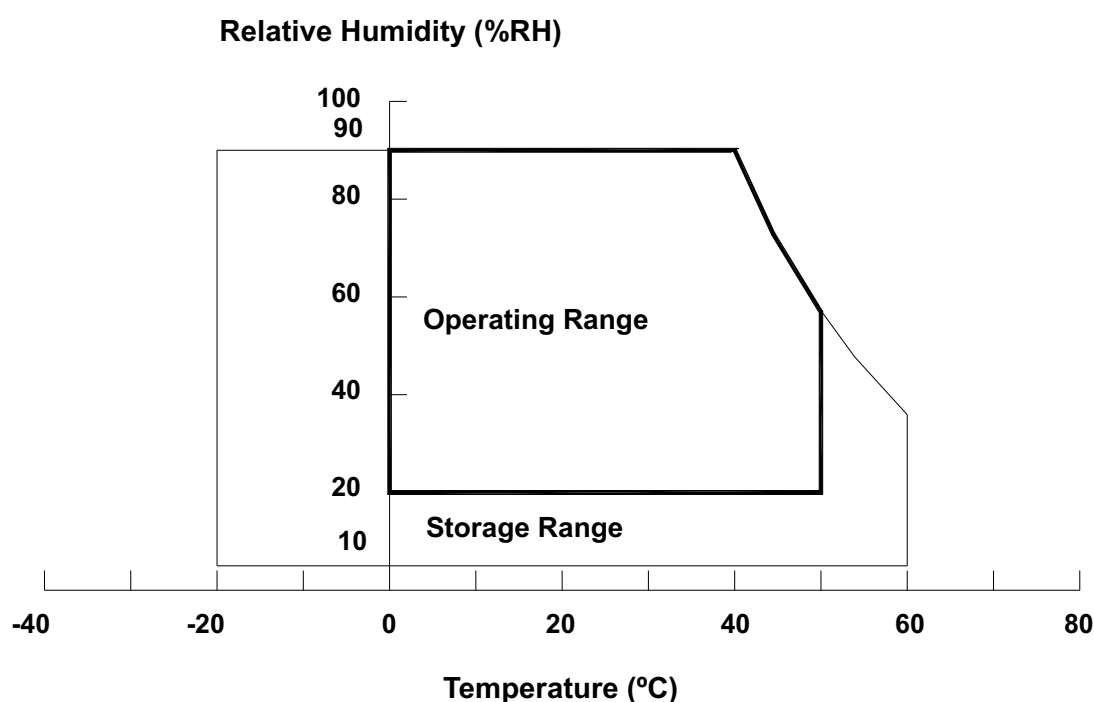
Temperature (ºC)

2.2 PACKAGE STORAGE

Storage Condition : With shipping package.

Storage temperature range : 25±5 ℃

Storage humidity range : 50±10%RH

Shelf life : a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

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3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	4.45	A	(2)
Power Supply Current	White Pattern	—	—	0.471	—	A	(3)
	Horizontal Stripe	—	—	0.852	1.015	A	
	Black Pattern	—	—	0.475	—	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$|V_{ID}|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

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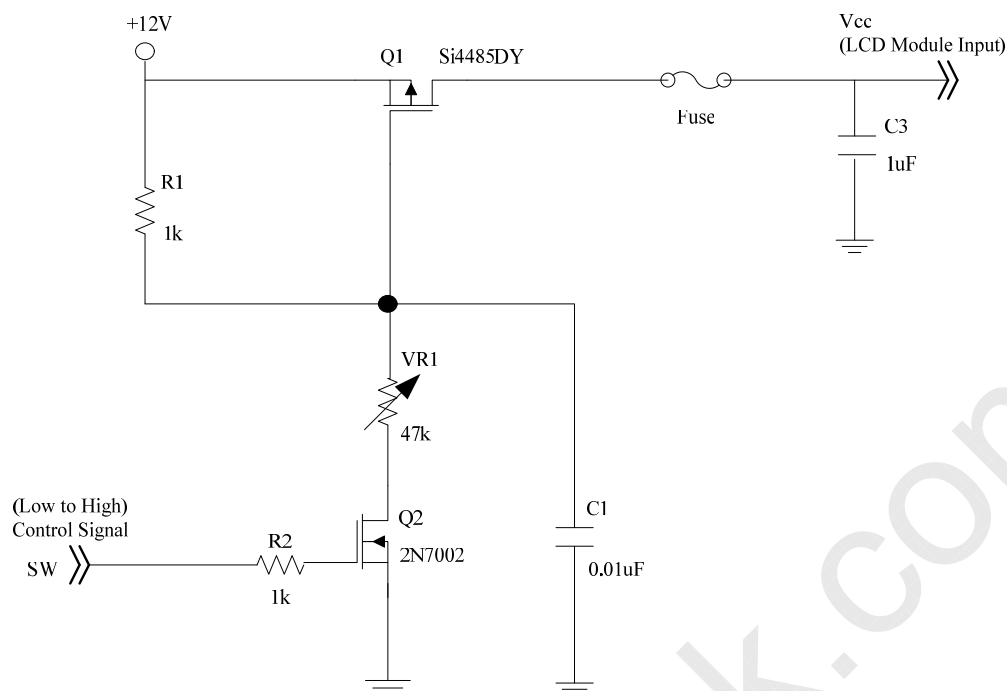
Vcc rising time is 470us
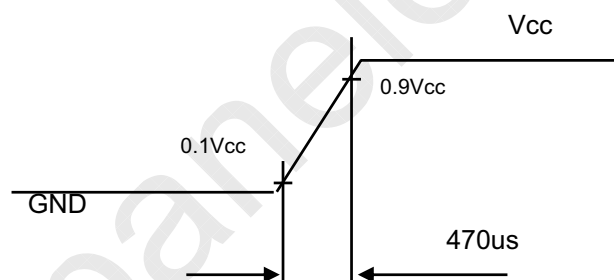
Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

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a. White Pattern

Active Area

b. Black Pattern

Active Area
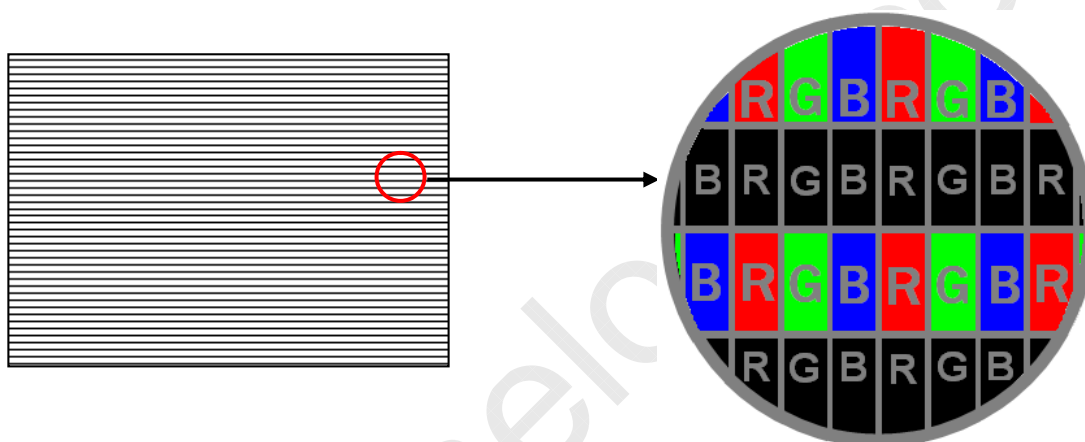
Note (4) The LVDS input characteristics are as follows:

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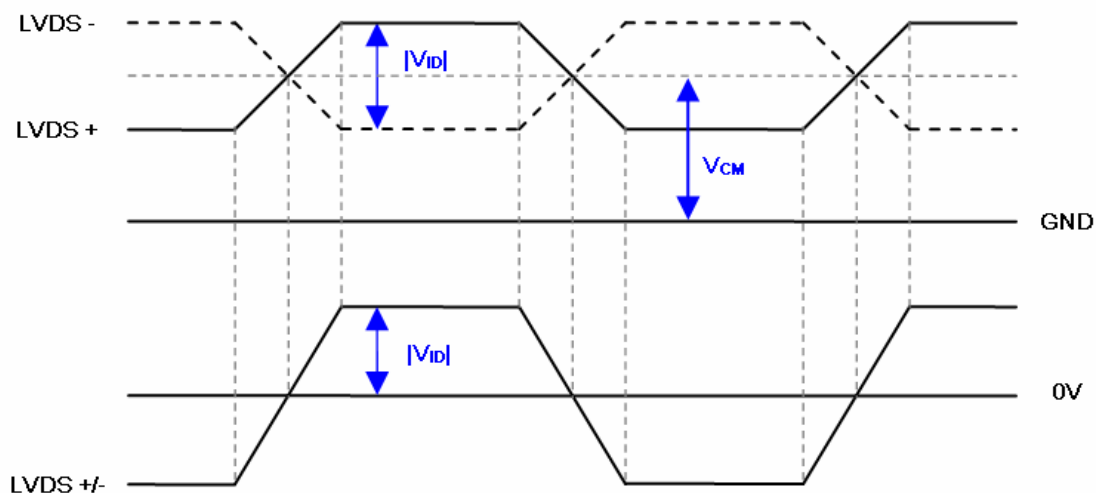
4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE

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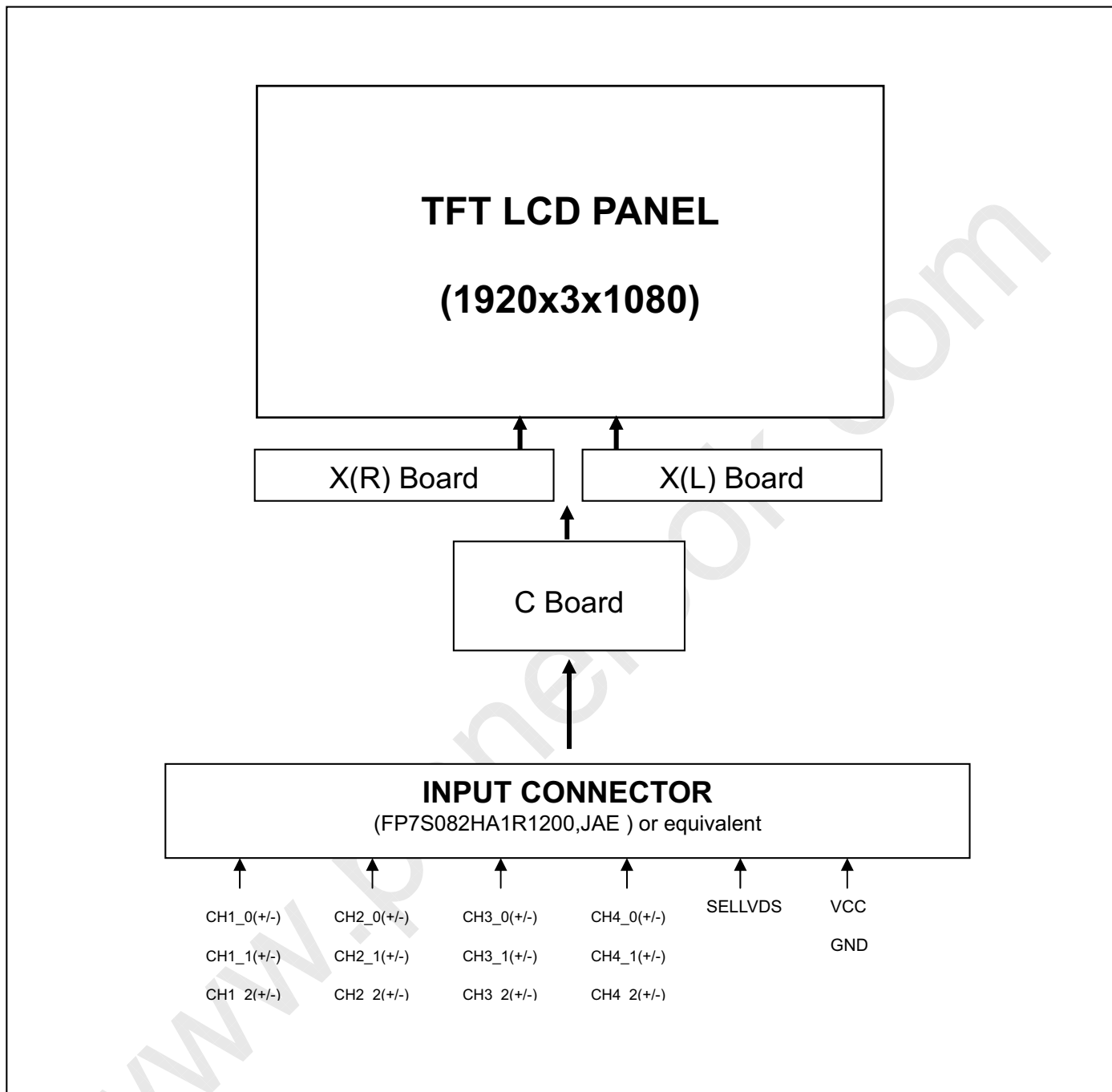
5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE INPUT

CNF1 Connector Pin Assignment (FP7S082HA1R1200,JAE Taiwan(台灣航空電子) or equivalent)

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	N.C.	No Connection	(1)
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
11	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
12	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
13	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
14	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
15	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH1CLK-	First pixel Negative LVDS differential clock input.	
18	CH1CLK+	First pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
21	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
22	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
23	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
26	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
27	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
28	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	

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29	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
30	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
31	GND	Ground	
32	CH3CLK-	Third pixel Negative LVDS differential clock input.	
33	CH3CLK+	Third pixel Positive LVDS differential clock input.	
34	GND	Ground	
35	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
36	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
37	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
38	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
39	GND	Ground	
40	SCL	I2C Bus	
41	3D_EN	3D Enable	(3)
42	LUT0	Look UP Table Select	(4)
43	Bus_EN	Bus Switch Enable	
44	SDA	I2C Bus	
45	LVDS_SEL	LVDS Data Format Selection	(2)
46	N.C.	No Connection	(1)
47	N.C.	No Connection	(1)
48	N.C.	No Connection	(1)
49	WP	Write Protection for EEPROM	
50	LUT1	Look UP Table Select	(4)
51	N.C.	No Connection	(1)
52	GND	Ground	
53	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
54	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
55	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
56	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
57	GND	Ground	
58	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
59	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
60	GND	Ground	

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61	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
62	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
63	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
64	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
65	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
66	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
67	GND	Ground	
68	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
69	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
70	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
71	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
72	GND	Ground	
73	CH2CLK+	Second pixel Positive LVDS differential clock input.	
74	CH2CLK-	Second pixel Negative LVDS differential clock input.	
75	GND	Ground	
76	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
77	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
78	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
79	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
80	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
81	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	
82	GND	Ground	

Note (1) Reserved for internal use. Please leave it open.

Note (2) High=connect to +3.3V : VESA Format ； Low= connect to GND or Open : JEIDA Format.

Note (3) High=connect to +3.3V : 3D mode ； Low= connect to GND or Open : 2D mode.

Note (4) Look up Table. Select

LUT1	LUT0	Table
0	0	2D OD
0	1	3D OD (High Temperature)

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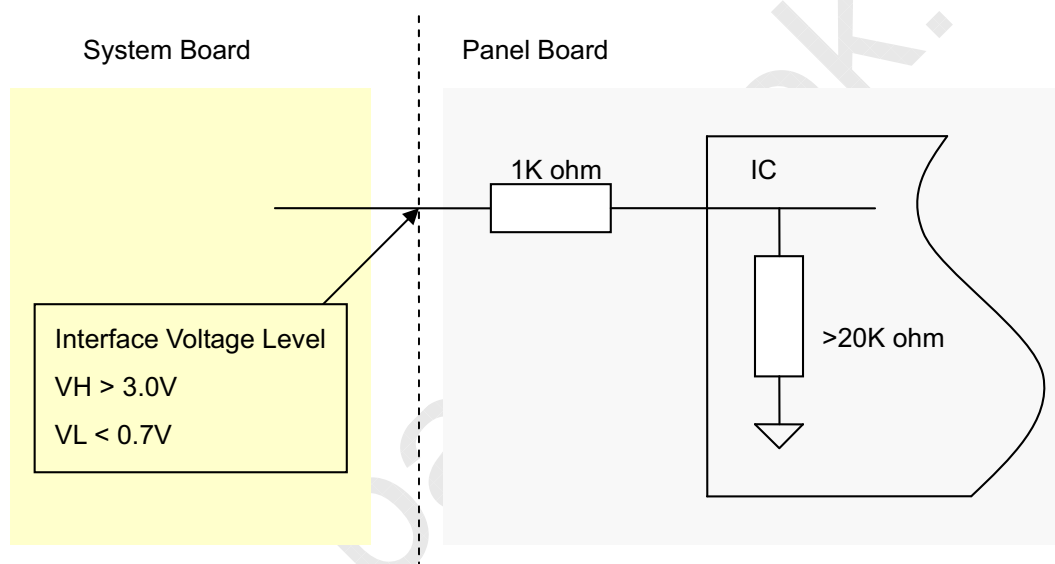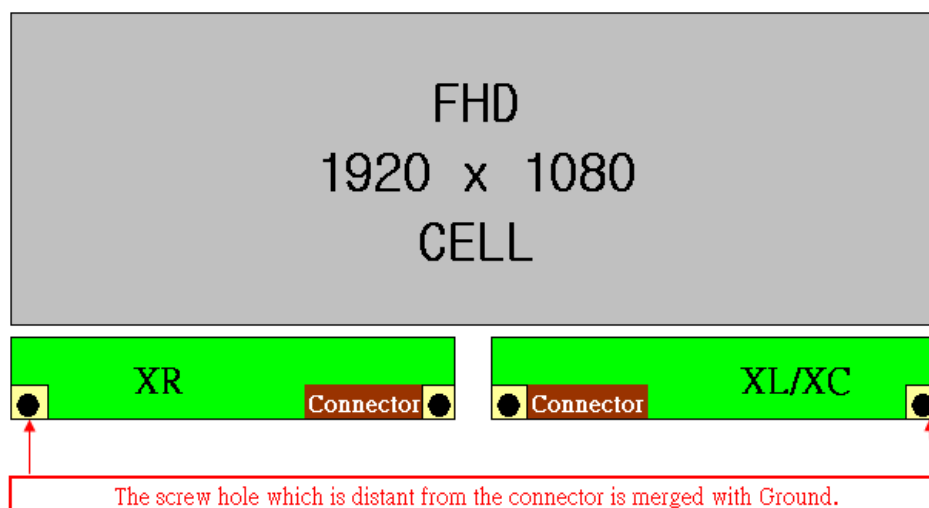|		
1	0	3D OD (Room Temperature)
1	1	3D OD (Low Temperature)

Note (5) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.

System Board　　　　　　　　Panel Board

1K ohm　　　IC

Interface Voltage Level
VH > 3.0V
VL < 0.7V

>20K ohm

Note (6) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

Note (7) The screw hole which is distant from the connector is merged with Ground

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5.2 LVDS INTERFACE

VESA Format : SELLVDS = H

JEIDA Format : SELLVDS = L or Open

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VESA Format

AR 0P / AR 0N	AR0	AG0	AR5	AR4	AR3	AR2	AR1	AR0	AG0
AR 1P / AR 1N	AG1	AB1	AB0	AG5	AG4	AG3	AG2	AG1	AB1
AR 2P / AR 2N	AB2	DE	VS	HS	AB5	AB4	AB3	AB2	DE
AR 3P / AR 3N	AR6	REV	AB7	AB6	AG7	AG6	AR7	AR6	REV
AR 4P / AR 4N	AR8	REV	AB9	AB8	AG9	AG8	AR9	AR8	REV

JEIDA Format

AR 0P / AR 0N	AR4	AG4	AR9	AR8	AR7	AR6	AR5	AR4	AG4
AR 1P / AR 1N	AG5	AB5	AB4	AG9	AG8	AG7	AG6	AG5	AB5
AR 2P / AR 2N	AB6	DE	VS	HS	AB9	AB8	AB7	AB6	DE
AR 3P / AR 3N	AR2	REV	AB3	AB2	AG3	AG2	AR3	AR2	REV
AR 4P / AR 4N	AR0	REV	AB1	AB0	AG1	AG0	AR1	AR0	REV

AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE　　: Data enable signal

DCLK : Data clock signal

RSV : Reserved

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color.

The higher the binary input, the brighter the color. The table below provides the assignment of the color versus

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data input.

Color		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
							Red									Green										Blue					
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:
	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:
	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:
	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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5.5 FLICKER (Vcom) ADJUSTMENT
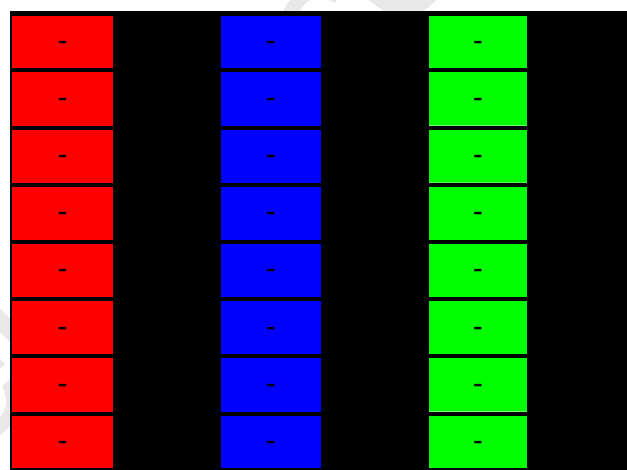
(1) Adjustment Pattern:

Flicker Pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.

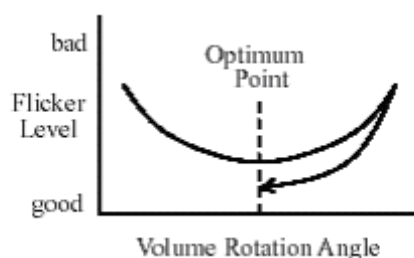Frame N   Frame N+1

(2) Adjustment method: (VR)

Flicker should be adjusted by turning the volume for flicker adjustment by the ceramic driver. It is adjusted to the point with least flickering of the center screen. After making it surely overrun at once, it should be adjusted to the optimum point.

(3) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

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6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

| Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	(5)
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	—	100	—	Hz	
		F_{r6}	—	120	—	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	540	550	575	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	—
	Blank	Thb	60	70	95	Tc	—

Note (1)　Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2)　Please make sure the range of pixel clock has follow the below equation:
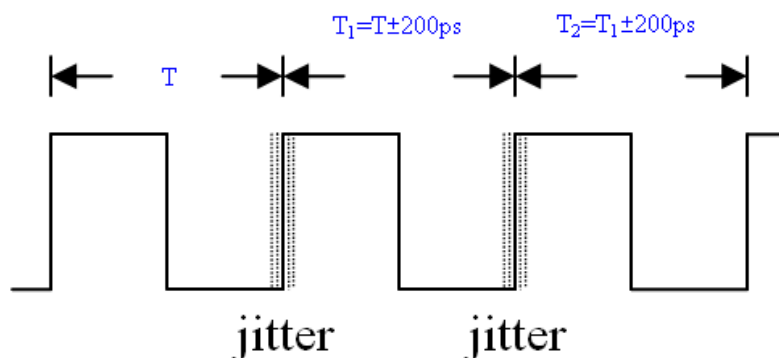
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$
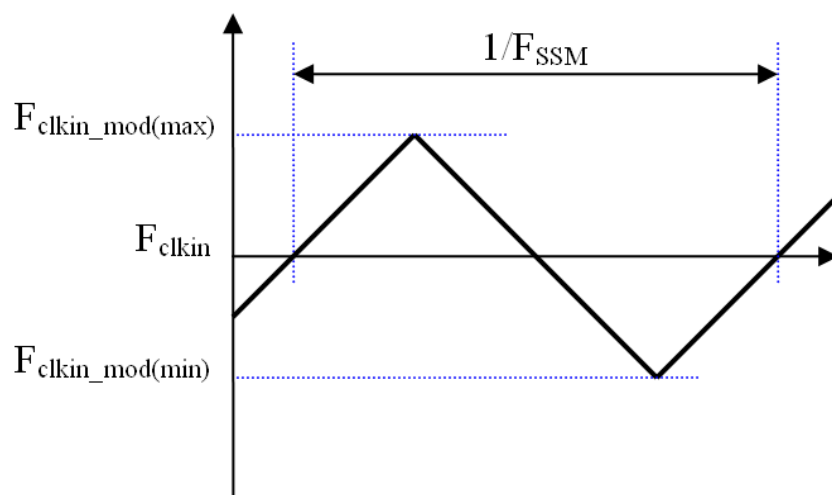
$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

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INPUT SIGNAL TIMING DIAGRAM
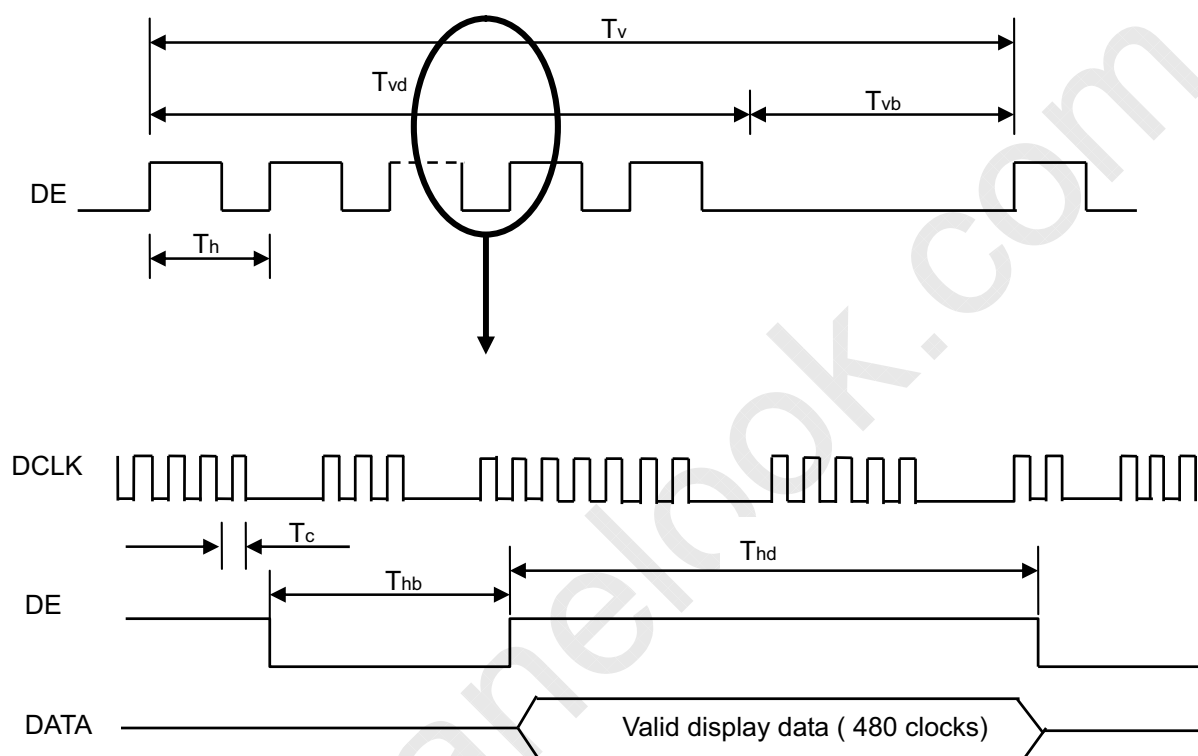
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

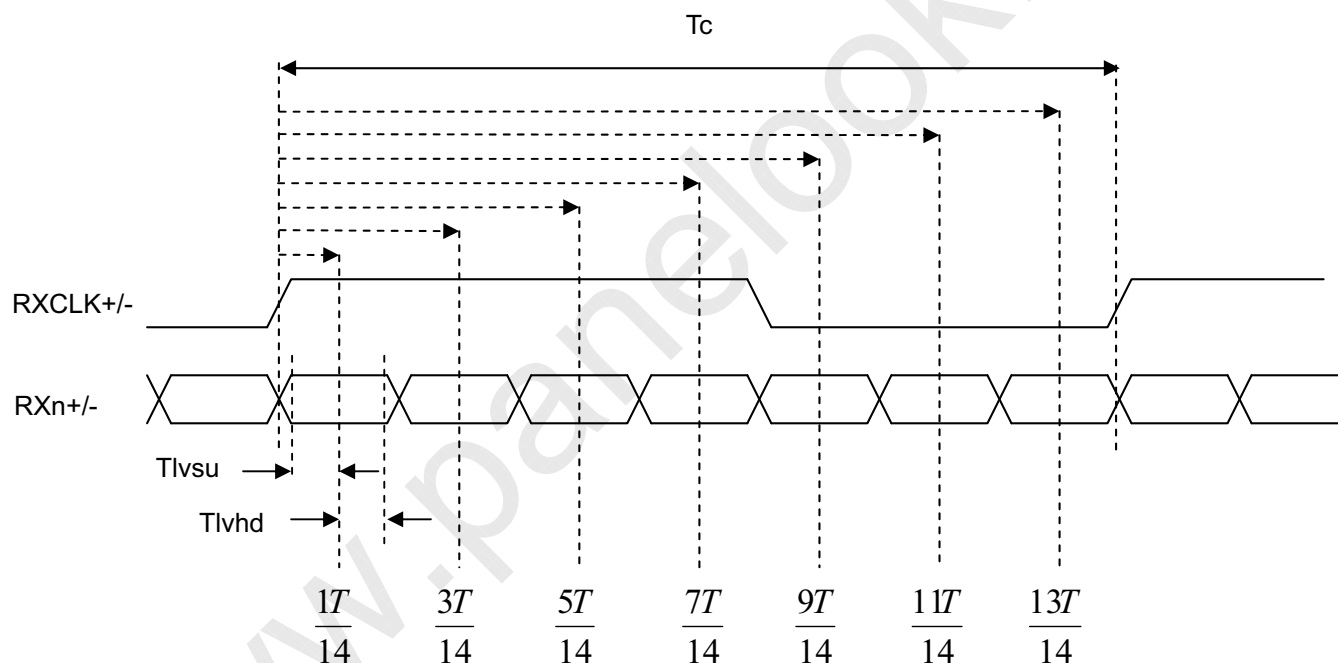Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.

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PRODUCT SPECIFICATION

$$1/F_{SSM}$$

$F_{clkin\_mod(max)}$

F_{clkin}

$F_{clkin\_mod(min)}$

Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM

Tc

RXCLK+/-

RXn+/-

Tlvsu

Tlvhd

$$\frac{1T}{14} \quad \frac{3T}{14} \quad \frac{5T}{14} \quad \frac{7T}{14} \quad \frac{9T}{14} \quad \frac{11T}{14} \quad \frac{13T}{14}$$

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ℃)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

Power ON/OFF Sequence
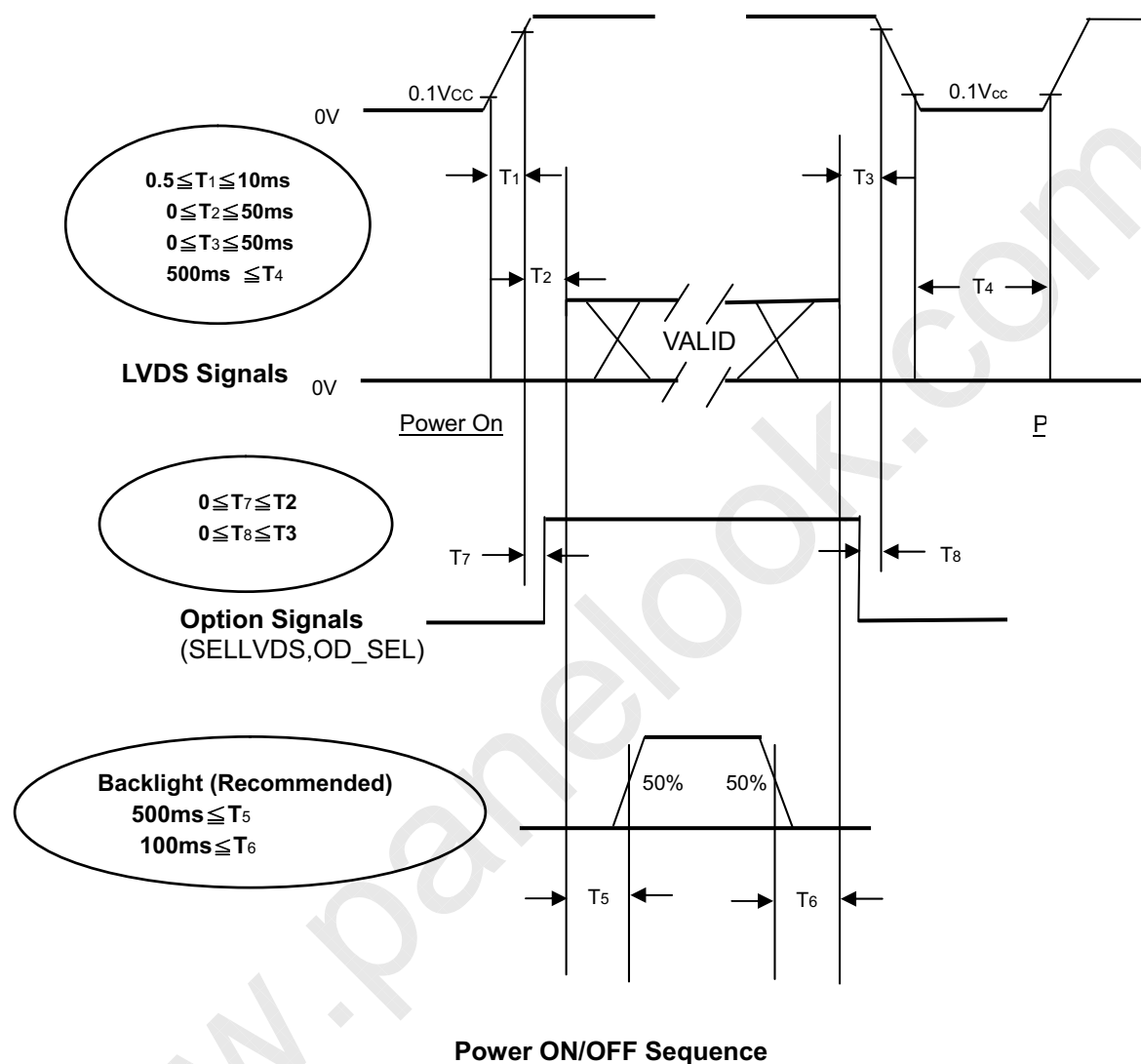
Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

PRODUCT SPECIFICATION

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	7.5 ± 0.5	mA
Oscillating Frequency (Inverter)	F_W	40 ± 3	KHz
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during

measuring in a windless room.

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PRODUCT SPECIFICATION
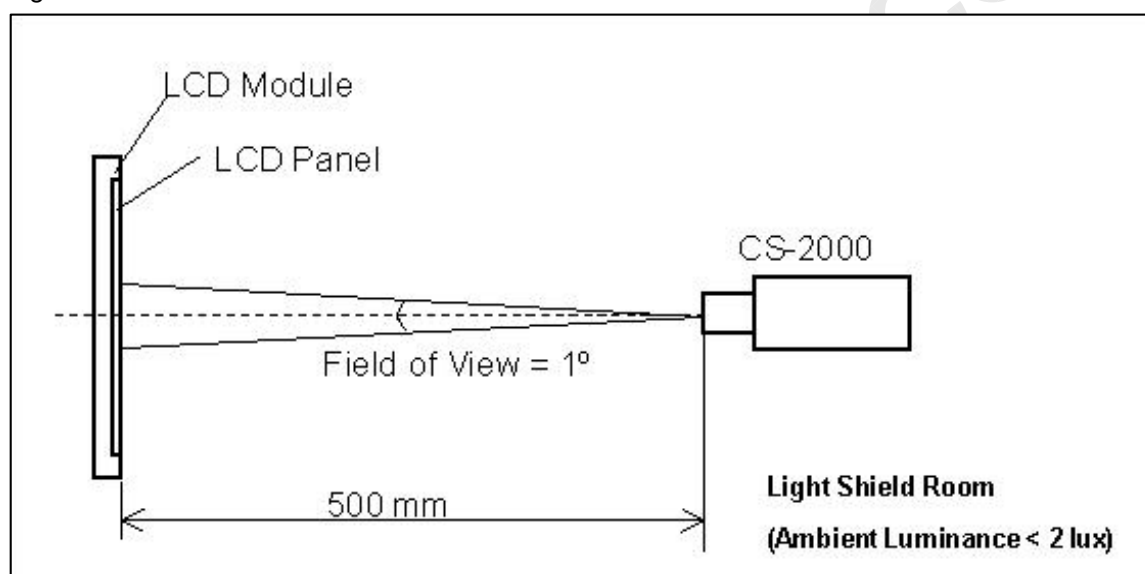
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

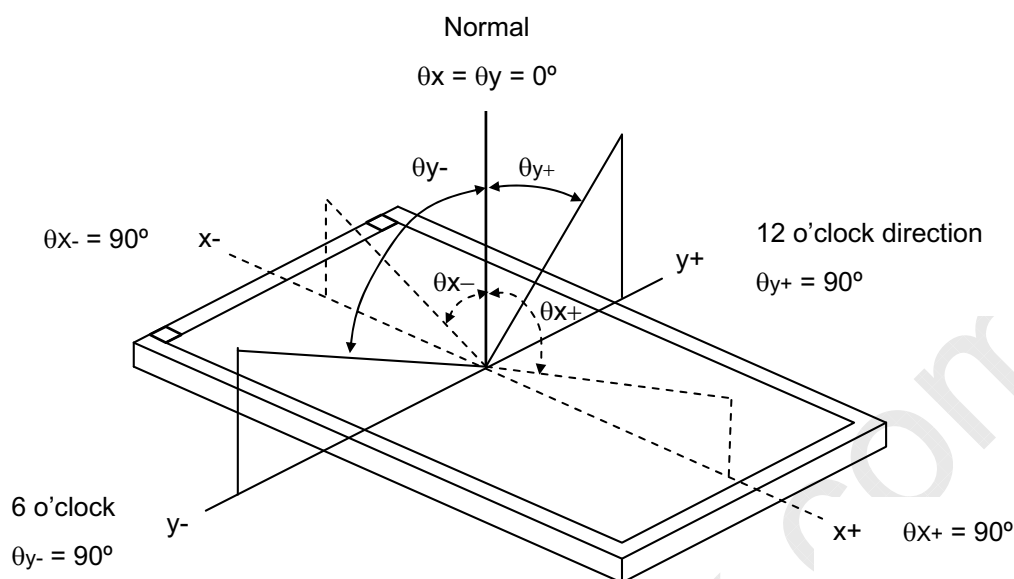| Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0°$, $\theta_Y=0°$ Viewing Angle at Normal Direction Standard light source "C"	-	0.657	-	-	(0),(1)
		Rcy			0.325		-	
	Green	Gcx			0.266		-	
		Gcy			0.591		-	
	Blue	Bcx			0.131		-	
		Bcy			0.115		-	
	White	Wcx			0.301		-	
		Wcy			0.357		-	
Center Transmittance		T%	$\theta_x=0°$, $\theta_Y=0°$ with CMI module	-	4.5	-	%	(1),(6)
Contrast Ratio		CR		4000	6000	-	-	(1),(3)
Response Time (VA)		Gray to gray	$\theta_x=0°$, $\theta_Y=0°$ with CMI Module@120Hz	-	6.5	12		(1),(4)
White Variation		δW	$\theta_x=0°$, $\theta_Y=0°$ with CMI module	-	-	1.3	-	(1),(5)
Viewing Angle	Horizontal	θ_x+	CR≥20 (VA) with CMI module		88		Deg.	(1),(2)
		θ_x-			88			
	Vertical	θ_Y+			88			
		θ_Y-			88			

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's W,R,G,B spectrum and BLU's spectrum. Which BLU (for V260H1-L03) is supplied by CMI.

2. Calculate cell's spectrum.

3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)

PRODUCT SPECIFICATION

Normal

$\theta x = \theta y = 0^\circ$

$\theta y-$ $\theta y+$

$\theta x- = 90^\circ$ x-

$\theta x-$

$\theta x+$

12 o'clock direction

$\theta y+ = 90^\circ$

y+

6 o'clock

y-

$\theta y- = 90^\circ$

x+ $\theta x+ = 90^\circ$

Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.
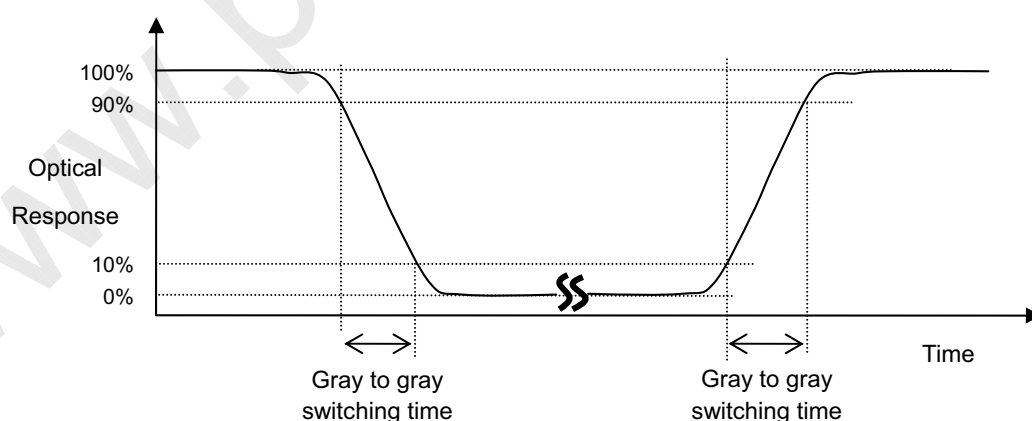
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Gray-to-Gray Switching Time:

100%
90%

Optical

Response

10%
0%

Time

Gray to gray
switching time

Gray to gray
switching time

The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

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Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

Horizontal Line

Active Area
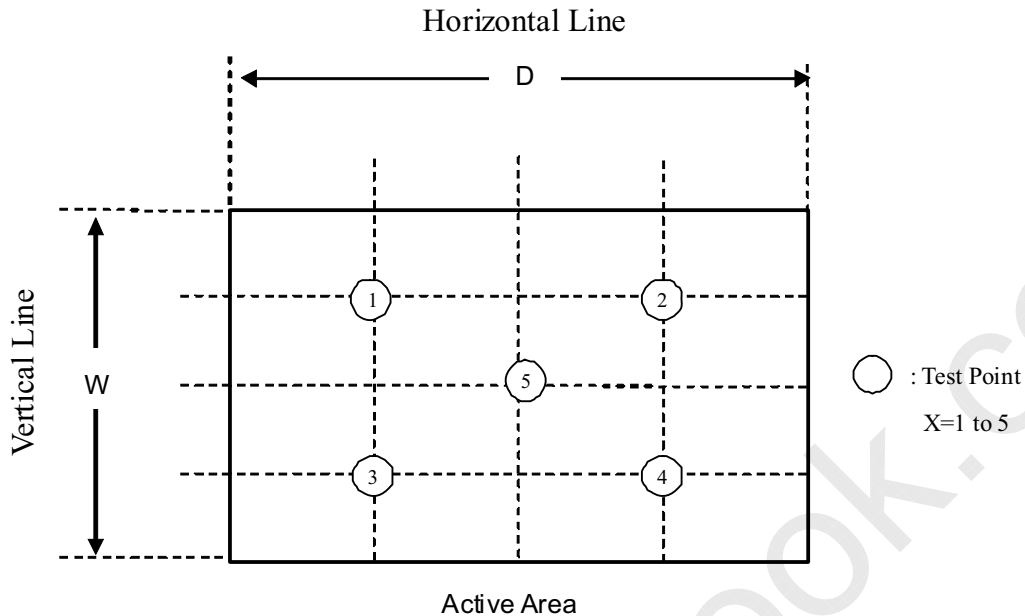
Note (6) Definition of Transmittance (T%) :

Measure the luminance of gray level 1023 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\% \text{ PRECAUTIONS}$$

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## 8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1]   Do not apply rough force such as bending or twisting to the module during assembly.

[2]   It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3]   Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4]   Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5]   The distance between COF edge and rib of BLU must bigger than 5mm. This can prevent the damage of COF when assemble the module.

[6]   Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.

[7]   If COF would bended to assemble in the module. Do not put the IC location on the bending corner of COF.

[8]   The gap between COF IC and any structure of BLU must bigger than 2mm. This can prevent the damage of COF IC

[9]   Bezel opening must have no burr. Burr will scrape the panel surface.

[10]   Bezel of module and bezel of set can not press or touch the panel surface. It will make light leakage or scrape.

[11]   When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.

[12]   The gap between Panel and any structure of Bezel must bigger than 2mm. This can prevent the damage of Panel.

[13]   Do not plug in or pull out the I/F connector while the module is in operation.

[14]   Do not disassemble the module.

[15]   Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[16]   Moisture can easily penetrate into LCD module and may cause the damage during operation.

[17]   When storing modules as spares for a long time, the following precaution is necessary.

    [17.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

    [17.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[18]   When ambient temperature is lower than 10ºC, the display quality might be reduced.
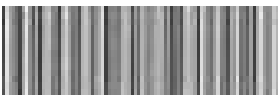
PRODUCT　SPECIFICATION

8.2 SAFETY PRECAUTIONS

[1]　The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2]　If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3]　After the module's end of life, it is not harmful in case of normal operation and storage.

PRODUCT SPECIFICATION

9. DEFINITION OF LABELS

9.1 OPEN CELL　LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

V315HK2-PE1 XX

XXXXXXXXXXXX
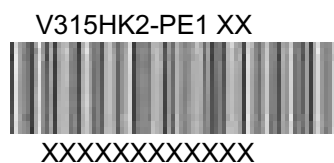
9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

P.O. NO.

Parts ID.

Model Name　　V315HK2-PE1

Carton ID.　　　　　　　　　Quantities　18

XXXXXXXXXXXXXX

Made In Taiwan

(a) Model Name: V315H3– PH1

(b) Carton ID: CM0 internal control

(c) Quantities: 18
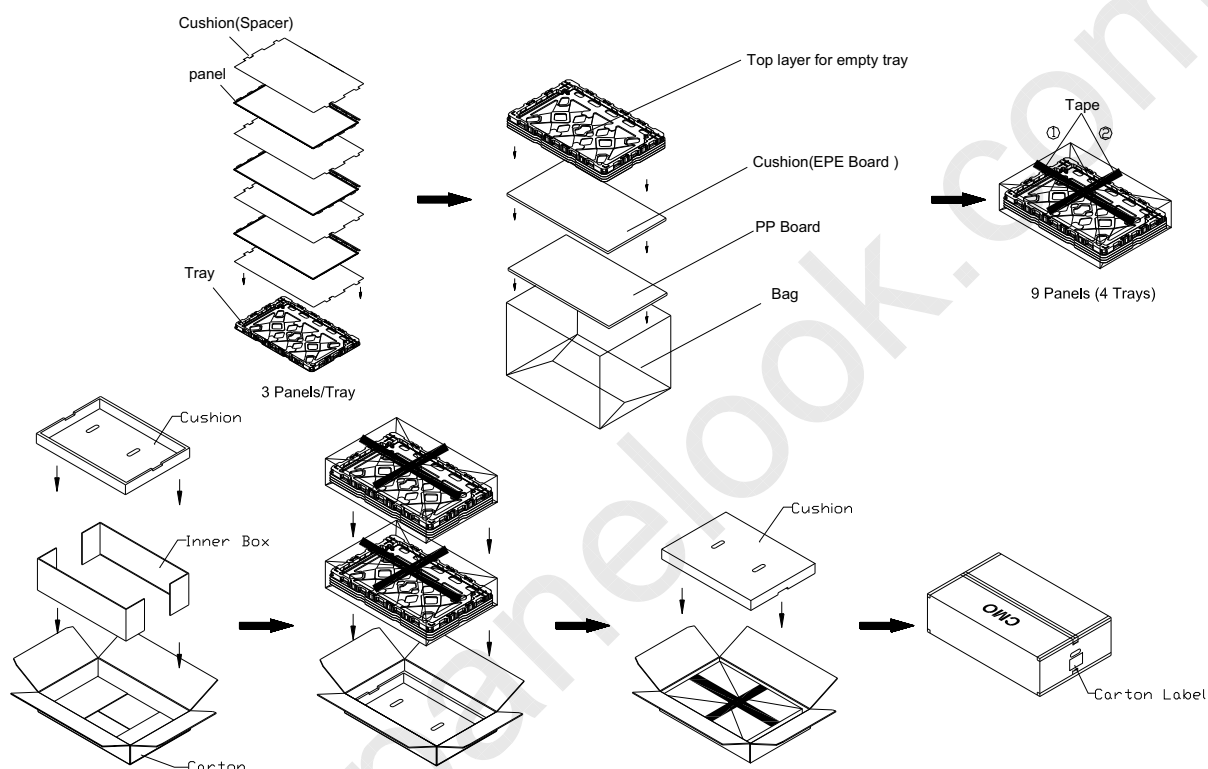
One step solution for LCD / PDP / OLED panel application: Datasheet, inventory and accessory! *www.panelook.com*

PRODUCT SPECIFICATION

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 18 LCD TV Panels / 1 Box

(2) Box dimensions : 970 (L) X 640 (W) X 319 (H)
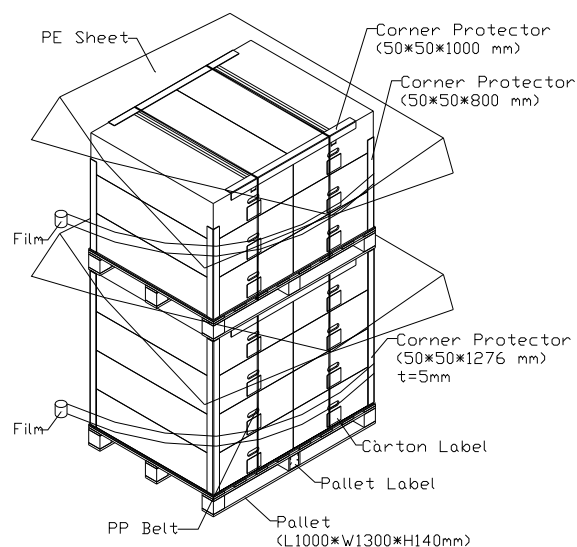
(3) Weight : approximately 36Kg (18 panels per box)

10.2 PACKAGING METHOD

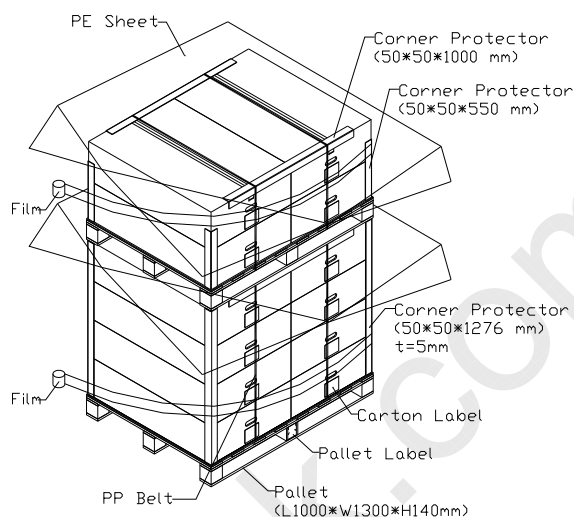Figures 10-1 and 10-2 are the packing method

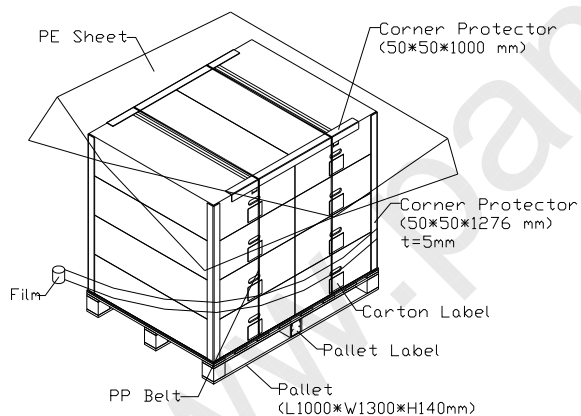One step solution for LCD / PDP / OLED panel application: Datasheet, inventory and accessory! *www.panelook.com*

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Sea / Land Transportation
(40ft HQ Container)

PE Sheet
Corner Protector
(50*50*1000 mm)
Corner Protector
(50*50*800 mm)
Film
Corner Protector
(50*50*1276 mm)
t=5mm
Film
Carton Label
Pallet Label
PP Belt
Pallet
(L1000*W1300*H140mm)

Sea / Land Transportation
(40ft Container)

PE Sheet
Corner Protector
(50*50*1000 mm)
Corner Protector
(50*50*550 mm)
Film
Corner Protector
(50*50*1276 mm)
t=5mm
Film
Carton Label
Pallet Label
PP Belt
Pallet
(L1000*W1300*H140mm)

Air Transportation

PE Sheet
Corner Protector
(50*50*1000 mm)
Corner Protector
(50*50*1276 mm)
t=5mm
Film
Carton Label
Pallet Label
PP Belt
Pallet
(L1000*W1300*H140mm)

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PRODUCT SPECIFICATION

11. MECHANICAL CHARACTERISTIC